LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

Features
- Internally trimmed offset voltage: 0.5 mV (max)
- Input offset voltage drift: 10 μV/°C (max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 3 MHz (min)
- High slew rate: 10 V/µs (min)
- Low supply current: 1.8 mA
- High input impedance: 10^12Ω
- Low total harmonic distortion: A_v 10, k_0.02%
- R_L 10k, V_O 20 Vp-p, BW 20 Hz - 20 kHz
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Typical Connection

Ordering Information
LF411XYZ
X indicates electrical grade
Y indicates temperature range
"M" for military
"C" for commercial
Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package

Dual-In-Line Package

Note: Pin 4 connected to case.

Order Number LF411ACH or LF411MH/883*
See NS Package Number H08A

*Available per JM38510/11904

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### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LF411A</th>
<th>LF411</th>
<th>H Package</th>
<th>N Package</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>±22V</td>
<td>±18V</td>
<td>670 mW</td>
<td>670 mW</td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>±38V</td>
<td>±30V</td>
<td>65°C/C/W (Still Air)</td>
<td>120°C/C/W</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range (Note 1)</td>
<td>±19V</td>
<td>±15V</td>
<td>2°C/C</td>
<td>2°C/C</td>
<td></td>
</tr>
<tr>
<td>Output Short Circuit Duration</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (Notes 2 and 9)</td>
<td></td>
<td></td>
<td>670 mW</td>
<td>670 mW</td>
<td></td>
</tr>
<tr>
<td>Tjmax</td>
<td>150°C</td>
<td>115°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>θA</td>
<td>162°C/C/W (Still Air)</td>
<td>120°C/C/W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>θC</td>
<td>20°C/C/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temp. Range (Note 3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temp. (Soldering, 10 sec.)</td>
<td></td>
<td></td>
<td>260°C</td>
<td>260°C</td>
<td></td>
</tr>
<tr>
<td>ESD Tolerance Rating to be determined.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

### DC Electrical Characteristics (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF411A</th>
<th>LF411</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VOS</td>
<td>Rg = 10 kΩ, T_A = 25°C</td>
<td>0.3</td>
<td>0.5</td>
<td>0.8</td>
</tr>
<tr>
<td>ΔVOS/ΔT</td>
<td>Average TC of Input Offset Voltage</td>
<td>Rg = 10 kΩ (Note 5)</td>
<td>7</td>
<td>10</td>
<td>7</td>
</tr>
<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>V_S = ± 15V (Note 4, 6)</td>
<td>25</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 25°C</td>
<td>2</td>
<td>2</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 70°C</td>
<td>25</td>
<td>25</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 125°C</td>
<td>50</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>V_S = ± 15V (Note 4, 6)</td>
<td>50</td>
<td>200</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 25°C</td>
<td>4</td>
<td>4</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 70°C</td>
<td>25</td>
<td>25</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_j = 125°C</td>
<td>50</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>RIN</td>
<td>Input Resistance</td>
<td>T_j = 25°C</td>
<td>10^12</td>
<td>10^12</td>
<td>Ω</td>
</tr>
<tr>
<td>AVOL</td>
<td>Large Signal Voltage Gain</td>
<td>V_S = ± 15V, V_O = ±10V, R_L = 2k, T_A = 25°C</td>
<td>50</td>
<td>200</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>Over Temperature</td>
<td>25</td>
<td>200</td>
<td>15</td>
<td>200</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>V_S = ± 15V, R_L = 10k</td>
<td>±12</td>
<td>±13.5</td>
<td>±12</td>
</tr>
<tr>
<td>VCM</td>
<td>Input Common-Mode Voltage Range</td>
<td>±16</td>
<td>±19.5</td>
<td>±11</td>
<td>±14.5</td>
</tr>
<tr>
<td></td>
<td>Common-Mode Rejection Ratio</td>
<td>Rg ≤ 10k</td>
<td>80</td>
<td>100</td>
<td>70</td>
</tr>
<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td>(Note 7)</td>
<td>80</td>
<td>100</td>
<td>70</td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current</td>
<td></td>
<td>1.8</td>
<td>2.8</td>
<td>1.8</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF411A</th>
<th>LF411</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>V_S = ± 15V, T_A = 25°C</td>
<td>10</td>
<td>15</td>
<td>8</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>V_S = ± 15V, T_A = 25°C</td>
<td>3</td>
<td>4</td>
<td>2.7</td>
</tr>
<tr>
<td>θn</td>
<td>Equivalent Input Noise Voltage</td>
<td>T_A = 25°C, Rg = 100Ω, f = 1 kHz</td>
<td>25</td>
<td>25</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>In</td>
<td>Equivalent Input Noise Current</td>
<td>T_A = 25°C, f = 1 kHz</td>
<td>0.01</td>
<td>0.01</td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>
Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\eta_A$.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. $V_{DSS}$, $I_B$, and $I_{OS}$ are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to ensure at least 90% of the units meet this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, $T_J$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, $P_D = T_J - T_{A} = \eta_A P_D$ where $\eta_A$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15V$ to $\pm 5V$ for the LF411 and from $\pm 20V$ to $\pm 5V$ for the LF411A.

Note 8: RETS 411X for LF411MH and LF411MJ military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

[Graphs and tables showing performance characteristics such as input bias current, supply current, common-mode input voltage limits, current limits, output voltage swing, etc.]
Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.
The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition.

When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

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Typical Applications (Continued)

10-Bit Linear DAC with No $V_{OS}$ Adjust

$$V_{OUT} = -V_{REF} \left( \frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots + \frac{A10}{1024} \right)$$

$-10V \leq V_{REF} \leq 10V$

$0 \leq V_{OUT} \leq \frac{-1023}{1024}V_{REF}$

where $A_N = 1$ if the $A_N$ digital input is high

$A_N = 0$ if the $A_N$ digital input is low

Single Supply Analog Switch with Buffered Output

Detailed Schematic
Physical Dimensions inches (millimeters)

Metal Can Package (H)
Order Number LF411MH/883 or LF411ACH
NS Package Number H08A

Ceramic Dual-In-Line Package (J)
Order Number LF411MJ/883
NS Package Number J08A
**LF411 Low Offset, Low Drift JFET Input Operational Amplifier**

**Physical Dimensions** inches (millimeters) (Continued)

![Physical Dimensions Diagram]

Molded Dual-In-Line Package (N)
Order Number LF411ACN or LF411CN
NS Package Number N08E

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